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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,339	12/11/2003	Seong-Hoon Lee	MIC-39	3691

1473 7590 12/17/2004

FISH & NEAVE LLP
1251 AVENUE OF THE AMERICAS
50TH FLOOR
NEW YORK, NY 10020-1105

EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,339	LEE, SEONG-HOON	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-20,22 and 27-35* is/are allowed.

6)☒ Claim(s) *1-8,21,23-26 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5-3-04* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-1-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21, 23-24 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 21, the limitation "said receiving", line 8, lacks antecedent basis.

In claim 23, the limitation "said input operative", line 20, lacks antecedent basis. Similar problem also occurs on line 26 of claim 36.

In claim 24, the limitation "said generated periodic reference signal", lines 21-22 and 23-24, lacks antecedent basis.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over PRIOR ART as shown in Fig. 1 (hereinafter, PA) in view of the Wu et al reference (U.S. Patent 6,100,736).

PA shows a DLL apparatus comprising a multiplexer 104; a delay line (101-103) having an input (XCLK), an output (BCLK); and a plurality of serially-connected unit delay elements (101-103), the output of said delay line being fed-back via said multiplexer to said delay line input to form a loop; said delay line loop operative to generate a periodic signal (BCLK) from at least the last one of said plurality of delay elements; a phase detector 107 having a first input operative to receive a periodic reference signal RCLK, a second input operative to receive said generated periodic signal, and an output, said detector operative to detect a phase difference between said periodic reference signal and said generated periodic signal; delay control logic (108) having an output and an input, said input to receive said phase detector output, said delay control logic operative to control a delay of delay elements; and logic operative (106) to activate said phase detector and said delay control logic and to enable said multiplexer after a plurality of cycles of said generated periodic signal (See description of Fig. 1) as partially required by claim 23.

PA does not disclose *a delay line having each unit delay element selectable to directly receive a delay line input signal* and *a delay control logic capable of selecting one of the unit delay elements* as specifically required by the claim.

Wu et al discloses in figure 1 and 5A-B a DLL apparatus comprising, among other things, *a delay line (130, details in 500) having each unit delay element (400) selectable to directly receive a delay line input signal (CLKIN)via means of control signals (ctrl0-n)* and *a delay control logic(120) capable of selecting one of the unit delay elements by providing control signals (ctrl0-n).*

It would have been obvious to one skilled in the art at the time the invention was made to replace a delay line in PA with the one taught by Wu et al since a delay line can be implemented in many different ways in the art.

A skilled artisan in the art would have selected a delay line taught by Wu et al since it is more compact and consuming less power.

As to claim 25, the scope of claim is similar to that of claim 23. Therefore, it is rejected for the same reason set forth above.

As to claim 26, figure 3 (and its description on col. 4) of Wu et al discloses cell of the shift register comprising a controllable inverter in which inverting function can be accomplished if and only if controllable inverter threshold is overcome. In other words, there is no changing in number of selecting unit delays if the phase difference is less than a certain value (i.e., threshold value).

As to claims 1-2, they are rejected for reciting methods/steps derived from the apparatus of claims 25-26 which are rejected.

As to claim 3, description of shift register in column 4 indicates that delay is shifted per unit. In other words, there is no changing of number of unit delays if the delay time is less than one unit delay.

As to claim 4, an inherent purpose of a DLL apparatus is to achieve a phase matching (i.e., phase different is zero degrees).

As to claim 5, col. 5, lines 1-4 of Wu et al discloses digitals signals including only one HIGH logic level signal, all others being LOW logic level signals.

As to claims 6 and 7, col. 5, lines 4-11 of Wu et al discloses selecting comprises selecting a higher number of said unit delays via digital signals when said phase difference is positive and selecting a lower number of said unit delays via digital signals when the phase difference is negative.

As to claim 8, the scope of claim is similar to that of claim 3. Therefore, it is rejected for the same reason set forth above.

5. Claim 36 is are rejected under 35 U.S.C. 103(a) as being unpatentable over the Lin reference (U.S. Patent 6,812,753) in view of the PRIOR ART as shown in Fig. 1 (hereinafter, PA) and further in view of the Wu et al reference (U.S. Patent 6,100,736).

Lin discloses in figure 6 an apparatus comprising a processor 302; a memory controller 330; plurality of DRAMs (col. 7, lines 2-5) having a DLL circuit as partially required by the claim.

Lin does not disclose a DLL circuit as specifically required by the claim (i.e., specific configuration of DLL recited in claim 23).

The combination of PA and Wu et al teachings meets the requirement of a specific configuration of the DLL circuit (See the rejection of claim 23 as noted above).

It would have been obvious to one skilled in the art at the time the invention was made to replace a DLL circuit in Lin with the one taught by PA in combination with Wu et al since a delay line can be implemented in many different ways in the art.

A skilled artisan in the art would have selected a delay line taught by PA in combination with Wu et al since it is more compact and consuming less power.

Allowable Subject Matter

6. Claims 9-20, 22 and 27-35 are allowed.

7. Claims 21 and 24 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus and method thereof comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the limitation *means for generating a first periodic signal with a first delay line and a second periodic signal with a second delay line* and *means for phase mixing the first and second generated periodic signals* as required by claims 24, 27, 21 and 9; and *means for phase mixing a first and a second periodic signal according to a first adjustable phase mixing ratio to produce a first phase-mixed signal; means for phase mixing said first and said second periodic signals according to a second adjustable phase mixing ratio to produce a second phase-mixed signal; means for phase mixing said first and said second phase mixed signals according to a third adjustable phase mixing ratio to produce a third phase-mixed signal; means for measuring said phase difference between said periodic reference signal and said third phase mixed signal after a plurality of cycles of said third phase mixed signal* as required by claims 35 and 22.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
12-08-04

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800